**ASSIGNMENT FRONT SHEET <No 2>**

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| **Qualification** | **Edexcel BTEC Level 5 HND Diploma in Computing and Systems Development** | | |
| **Unit number and title** | **Unit 51: Computer Systems Architecture** | | |
| **Assignment due** |  | **Assignment submitted** | 2 |
| **Learner’s name** |  | **Assessor name** | Hoang Duc Quang |

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| **Learner declaration:**  I certify that the work submitted for this assignment is my own and research sources are fully acknowledged. | | | |
| **Learner signature** |  | **Date** |  |

**Grading grid**

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| P5 | P6 | P7 | P8 | P9 | M2 | M3 | D1 | D2 |
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| **Assignment title** | **Computer Systems Architecture** | | | |
| In this assignment, you will have opportunities to provide evidence against the following criteria.  Indicate the page numbers where the evidence can be found. | | | | |
| **Assessment criteria** | | **Expected evidence** | **Task no.** | **Assessor’s Feedback** |
| **LO2. Understand the functions of computer system components** | | | | |
| P5.illustrate the key computer system components and how they interact | |  | Task 3 |  |
| P6.explain the different types of memory that can be attached to a processor | |  | Task 3 |  |
| P7. explain how polling and  interrupts are used to allow  communication between  processor and peripherals | |  | Task 3 |  |
| **LO3. Understand the principles of processor operations.** | | | | |
| P8.compare Reduced InstructionSet Computer (RISC) chipsand Complex Instruction SetComputer (CISC) chips | |  | Task 4 |  |
| P9.illustrate the use of the  different processor registers  in the fetch-execute cycle. | |  | Task 4 |  |

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| **Assessment criteria** | **Expected Evidence** | **Feedback**  **(note on Merit/Distinction if applicable)** |
| **M2**compare the roles played by different types of memory |  |  |
| **M3**create a low-level program which includes decision making and branching. |  |  |
| **D1**explain how the processor is physically connected to memory and input/output (I/O) devices using the system buses. |  |  |
| **D2**explain how the width of the data bus and address bus affect processor performance and complexity. |  |  |

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| Summative feedback | | | |
| **Assessor’s Signature** |  | Date |  |

**<ATTACHED EVIDENCE>**